REMARKS/ARGUMENTS

Reconsideration is requested of all rejections based on 35 USC 112:

Claim 1 has been rejected under 35 USC 112, first paragraph, as "failing to comply with the written description requirement.....Claim 1 recites the limitation of 'with no intervening steps'. There is no positive support for this limitation in the specification..."

We believe that this is incorrect. In detailing the written description requirement, the MPEP (section 2163) states "The subject matter of the claim need not be described literally (i.e., using the same terms or *in haec verba*) in order for the disclosure to satisfy the description requirement." The question that needs to be answered is 'what would be a reasonable interpretation of what is taught in the specification'. Absent an explicit qualification to the contrary, the normal meaning of a statement that a given step is followed by a second step, is that there are no intervening steps. To suppose otherwise, would imply that, whenever a sequence of steps is recited, it can be assumed that there are other intermediate steps unless the absence of such steps is explicitly stated. Such an assumption is, however, clearly invalidated by section 2163, as quoted above.

Reconsideration is requested of all rejections based on 35 USC 102:

Claims 1-2 have been rejected under 35 USC 102 as being anticipated by Narwanker et al. Examiner argues that, in col. 13 line 65 to col. 14 line 4 Narwanker teaches applying a low power level only to a plasma. This is incorrect. Bias power is also applied, as well as plasma power. Examiner is similarly incorrect in quoting col. 14 lines

Appl. No. 09/579,542

Amdt. dated September 2 2003

Reply to Office action of June 11 2003

11-29 as teaching applying a high power level only to a plasma. Examiner then argues that the step of repeating the low and high power depositions is also taught by Narwanker because his flowchart (FIG. 8B) shows a return connection from the final step back to the first step. This is also incorrect because the last step is 'remove wafer from system' which clearly implies a fresh wafer for each pass through the chart. Also, returning to the first step of the chart means "going through all steps in the process" not "repeating the preceding two steps" as recited in our claim 1.

Reconsideration is requested of all rejections based on 35 USC 103:

Claims 6-7 have been rejected under 35 USC 103 as being anticipated by Narwanker et al. in view of Moghadam. The latter is cited because he teaches (in two different embodiments) low and high power levels in the ranges we claim. This is little different from Examiner stating that films can be deposited at any power level one desires! He has completely separated the ranges claimed in 6 and 7 from the context in which they are to be applied (namely claim 1).

Claim 8 has been rejected under 35 USC 103 as being unpatentable over Narwanker et al. in view of Huang et al. One of the most important teachings of the present invention is that flat band voltages as low as -3V can be achieved (if our process is used). In an earlier office action, Examiner had argued that, since silica is known to have a flat band voltage of -1.82V, -3V is not an improvement over the prior art. We pointed out that -3V was much lower than had been reported for films (as opposed to bulk). Examiner now quotes Huang as reporting that -15V is a "typical and acceptable value for flat band voltage" and argues that this makes -3V obvious!. This is like arguing

Appl. No. 09/579,542

Amdt. dated September 2 2003

Reply to Office action of June 11 2003

that a sailboat capable of doing 100 knots is not novel since power boats can do 200 knots and 15 knots is typical and acceptable for most sailboats.

Claims 9-13 have been rejected under 35 USC 103 under Moghadam in view of Murugesh. As in (c) above Moghadam is cited as teaching (in different embodiments) use of low and high power while Murugesh is relied on as teaching repeating the steps. As we have pointed out in earlier correspondence, Murugesh's repeated application of power is to the substrate (specifically to heat it **while the plasma is off**) and not to the plasma.

Finally, we respectfully restate for examiner's review the four basic considerations, that apply to obviousness rejections, ALL of which must be met (as enunciated in section 2141 of the MPEP):

(1) The claimed invention must be considered as a whole:

The invention is a process for depositing, through plasma enhanced chemical vapor deposition, inorganic films having low dielectric constant. In addition, the process of the present invention teaches how to form low k films that have a flat band voltage of -3V. The patent literature is extensive enough that virtually any invention can be constructed by combining steps that have already been described as part of other inventions. This is not sufficient to demonstrate lack of novelty in this case since examiner has cited no inventions that claim to have produced THIN FILMS (not bulk material) having the dielectric properties that we claim.

(2) The references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination:

Appl. No. 09/579,542

Amdt. dated September 2 2003

Reply to Office action of June 11 2003

None of the references cited by examiner suggest that their teachings could be combined with others to produce the result disclosed by the present invention.

(3) The references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention:

The only reason examiner has for selecting the particular process steps that he uses to construct the present invention is that (in his view) they would, when combined, constitute the present invention. This is hindsight.

(4) Reasonable expectation of success is the standard with which obviousness is determined:

There is nothing in any of the cited references, taken singly or together, that gives one reason to expect the outcome disclosed by the present invention. In fact, in rejecting claim 8, Examiner quotes Huang as stating that -15V is a "typical and acceptable value for flat band voltage" which is a clear indication that the value of -3V claimed by the present invention is unexpected as far as the prior art is concerned.

For the above reasons, applicant respectfully requests that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

GEO. O. SAILE & ASSOCIATES

28 Davis Avenue

Poughkeepsie NY 12603

_ 7700

George O. Saile

Reg. No. 19572

Page 10 of 10